PATENT

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Akio SUGI, *et al.*

Patent No.: 7,034,377 B2
Issued April 25, 2006

Serial No.: 10/720,738
Filed: November 24, 2003
Title: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING...
Group Art Unit: 2814
Examiner: Rao, Shrinivas H.
Attorney Docket No.: FUJI:280

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REQUEST FOR CERTIFICATE OF CORRECTION

Sir:

Applicants request that a Certificate of Correction be issued to correct errors that appear in the above-referenced patent due to mistakes made on the part of the Office, namely, typographical errors in Claims 10 and 11. For the convenience of the Office, Applicants enclose the claims portion of the amendment filed on March 11, 2005 indicating how the claims should read. Claims 15 and 17 in the Amendment correspond to claims 10 and 11, respectively, in the Issued Patent. Form PTO/SB/44, indicating the corrections as requested, is submitted herewith. Applicants request that a Certificate of Correction be issued to make this correction.

In the event that it should be determined that the error is not the fault of the Office, the Commissioner is authorized to charge deposit account 18-2056 any fees associated with the issuance of the Certificate of Correction.

Respectfully submitted,

ROSSI, KIMMS & McDOWELL LLP

06/20/06
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IN THE CLAIMS

The status of the claims as presently amended is as follows:

1. (*Currently Amended*) A semiconductor device comprising:

a semiconductor substrate;

a trench formed in the substrate;

at least one non-trench region surrounded by the trench;

~~an~~a plurality of active regions formed on the substrate over the trench, each for driving current as a semiconductor element;

a first diffusion region formed at a bottom of the trench in the active regions; and

a second diffusion region formed in the non-trench region,

wherein current is flowable between the first diffusion region and the second diffusion region,

wherein the trench comprises a plurality of first trench sections formed in the active regions, and a plurality of second trench sections intersecting the first trench sections to form a mesh pattern surrounding the non-trench region,

wherein the first diffusion region is formed at the bottom of the first ~~and second~~ trench sections, and

wherein the trench further includes at least one third trench section connected to the first or second trench sections or both the first and second trench sections to divide the non-trench region into a plurality of smaller regions,

wherein a first conductor is formed with an insulator film interposed therebetween in the first, second, and third trench sections, and

wherein the width of each of the second and third trench sections is smaller than the width of each of the first trench sections.

2. (*Canceled*)

3. (*Currently Amended*) The semiconductor device as claimed in claim [[2]]1, further including:

an electrode electrically connected to the second diffusion region; and

a contact section electrically connected to the second diffusion region and the electrode,

wherein the contact section is disposed over and contacting all of the smaller regions in the non-trench region.

4. (*Currently Amended*) The semiconductor device as claimed in claim [[2]]1, wherein the third trench section extends parallel to the first trench sections.

5. (*Currently Amended*) The semiconductor device as claimed in claim [[2]]1, wherein the third trench section extends parallel to the second trench sections.

6. (*Currently Amended*) The semiconductor device as claimed in claim [[2]]1, wherein the third trench section extends diagonally to both the first and second trench sections.

7. (*Currently Amended*) The semiconductor device as claimed in claim [[2]]1, wherein the third trench section comprises a combination of two or three subsections, each of which extends parallel to the first trench sections, parallel to the second trench sections, or diagonally to both the first and second trench sections.

8. (*Currently Amended*) ~~The~~A semiconductor device ~~as claimed in claim 2,~~comprising:

a semiconductor substrate;

a trench formed in the substrate;

at least one non-trench region surrounded by the trench;

an active region formed on the substrate over the trench for driving current as a semiconductor element;

a first diffusion region formed at a bottom of the trench in the active region; and

a second diffusion region formed in the non-trench region,

wherein current is flowable between the first diffusion region and the second diffusion region,

wherein the trench comprises a first trench section formed in the active region, and a

second trench section intersecting the first trench section to form a mesh pattern surrounding the non-trench region,

wherein the first diffusion region is formed at the bottom of the first trench section, and

wherein the semiconductor device is a trench lateral transistor composed of at least the semiconductor substrate, the first and second diffusion regions, the first diffusion region driving current as a transistor, a gate insulator film formed inside the trench, a first conductor formed inside the gate insulator film, a second conductor formed inside the first conductor in the active region with an interlayer insulator film interposed therebetween and electrically connected to the first diffusion region, a first electrode penetrating through the interlayer insulator film electrically connected to the second diffusion region, and a second electrode penetrating through the interlayer insulator film to electrically connect to the second conductor.

9-12. (*Canceled*)

13. (*Currently Amended*) The semiconductor device as claimed in claim [[8]]1, wherein the second diffusion region is a drain region and the first diffusion region is a source region.

14. (*Currently Amended*) The semiconductor device as claimed in claim [[8]]1, wherein the second diffusion region is a source region and the first diffusion region is a drain region.

15. (*Currently Amended*) The semiconductor device as claimed in claim [[13]]1, further including a first electrode electrically connected to the second diffusion region, wherein the inside of the third trench section is filled with the first conductor with [[the]]a gate insulator film interposed therebetween, and the first conductor in the third trench section and the first electrode are insulated from each other by an interlayer insulator film.

16. (*Canceled*)

17. (*Currently Amended*) The semiconductor device as claimed in claim [[8]]25, wherein an

interlayer insulator film thicker than the gate insulator film is provided along a part of a side section of the first trench sections.

18-20. (*Canceled*)

21. (*Currently Amended*) The semiconductor device as claimed in claim [[19]]1, further including an interlayer insulator film thicker than the insulator film in each of the first trench sections and the second trench sections on each side section of the first trench sections and on each side section or at a bottom of the second trench sections.

22. (*Canceled*)

23. (*Currently Amended*) A method of manufacturing a semiconductor device comprising a semiconductor substrate, a trench formed in the substrate, ~~an~~a plurality of active regions formed on the substrate over the trench, each for driving [[a]] current as a semiconductor element, at least one non-trench region surrounded by the trench, a first diffusion region formed on the trench, and a second diffusion region formed in the non-trench region, wherein current is flowable between the first diffusion region and the second diffusion region, wherein the trench comprises a plurality of first trench sections formed in the active regions and a plurality of second trench sections intersecting the first trench section to form a mesh pattern surrounding the non-trench region, wherein the trench further includes at least one third trench section connected to the first or second trench sections or both the first and second trench sections to divide the non-trench region into a plurality of smaller regions, wherein a first conductor is formed with an insulator film interposed therebetween in the first, second, and third trench sections, and wherein the width of each of the second and third trench sections is smaller than the width of each of the first trench sections, the method comprising the steps of:

forming the first and second trench sections on the semiconductor substrate;

forming the first diffusion region on each of the bottom of the first ~~and second~~ trench sections;

filling the first trench and the second trench; and

forming the second diffusion region in the non-trench region.

24. (*New*) A semiconductor device comprising:

a semiconductor substrate;

a trench formed in the substrate;

at least one non-trench region surrounded by the trench;

a plurality of active regions formed on the substrate over the trench, each for driving current as a semiconductor element; and

a first diffusion region and a second diffusion formed at a bottom of the trench in the active regions,

wherein current is flowable between the first diffusion region and the second diffusion region,

wherein the trench comprises a plurality of first trench sections formed in the active regions, and a plurality of second trench sections intersecting the first trench sections to form a mesh pattern surrounding the non-trench region,

wherein the first and second diffusion regions are formed at the bottom of the first and second trench sections, respectively,

wherein a first conductor is formed with an insulator film interposed therebetween in the first and second trench sections, and

wherein the width of each of the second trench sections is smaller than the width of each of the first trench sections.

25. (*New*) The semiconductor device as claimed in claim 1, further including a second conductor electrically connected to the first diffusion region with an interlayer insulator film interposed therebetween inside the first conductor in the first trench sections.

26. (*New*) The semiconductor device as claimed in claim 24, further including a second conductor electrically connected to the first diffusion region with an interlayer insulator film

interposed therebetween inside the first conductor in the first trench sections.

27. (*New*) The semiconductor device as claimed in claim 24, wherein the second diffusion region is a drain region and the first diffusion region is a source region.

28. (*New*) The semiconductor device as claimed in claim 24, wherein the second diffusion region is a source region and the first diffusion region is a drain region.

29. (*New*) The semiconductor device as claimed in claim 24, further including an interlayer insulator film thicker than the insulator film in each of the first trench sections and the second trench sections on each side section of the first trench sections and on each side section or at a bottom of the second trench sections.

PTO/SB/44 (04-05)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,034,377 B2

APPLICATION NO.: 10/720,738

ISSUE DATE : November 24, 2003

INVENTOR(S) : Akio SUGI et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Column 32, Line 55 (in Claim 10) the phrase "further including at first electrode" should be replaced with:
--further including a first electrode--

In Column 32, Line 57 (in Claim 10) the phrase "conductor a with gate" should be replaced with:
--conductor with a gate--

In Column 32, Line 61 (in Claim 11) the phrase "as claimed in claim 1" should be replaced with:
--as claimed in claim 15--

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